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PATENT
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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1-20 remain.

Claims 1-8, 10, and 14 - 20 are being cancelled.

Claims 9, 11, and 12 are being amended.

WHAT IS CLAIMED IS:

1. – 8. (Cancelled)

9. (Currently Amended) A clock signal generator comprising:

a phase detector for comparing a digital input clock signal with a reference signal to generate a digital phase detection signal;

circuitry for generating a memory index from said digital phase detection signal;

a memory storing digital data representing real and imaginary parts of a digital complex waveform accessible by said memory index;

a digital to analog converter for converting digital data accessed from said memory into an analog complex waveform, the digital to analog converter comprising:

low pass filters for filtering said real and imaginary parts of said digital complex waveform;

a rotator for rotating said real and imaginary parts of said digital complex waveform by a selected angle such that a noise shaping function of said digital to

analog converter tracks a center frequency of said digital output clock; and

quantizers for generating said real and imaginary parts of said analog complex waveform from rotated real and imaginary parts output from said rotator;

bandpass filters for filtering the analog complex waveform to reduce jitter in a binary clock signal derived therefrom; and

a phase locked loop for generating the binary clock signal from said analog complex waveform and a complex reference signal, wherein the binary clock signal has a rate near an integer multiple of a rate of said analog complex waveform.

10. (Cancelled)

11. (Currently Amended) The clock signal generator of Claim 9 [[10]] wherein said digital to analog converter further comprises a feedback loop including a second rotator for feeding back a rotated output of said quantizer to inputs of said low pass filters.

12. (Currently Amended) The clock signal generator of Claim 9 [[10]] wherein said bandpass filters each comprise at least one continuous time filter stage.

13. (Previously Presented) The clock signal generator of Claim 12 wherein said continuous time filter stages comprises at least one resonator including at least one variable transconductance.

14. – 20. (Cancelled)